REMARKS

Status Summary

Claims 1-14 are pending in the present application. Claims 5-12 have been allowed, and claims 1-4, 13, and 14 presently stand rejected. Reconsideration of the application based on the remarks set forth hereinbelow is respectfully requested.

Specification

The Examiner has stated that the abstract of the disclosure is objected to because of the use of the term "comprising" on line 3. The Examiner suggested that the term "comprising" should be replaced with the term "including". This change has been made to the specification as indicated by the amendment above.

Claim Rejection - 35 U.S.C. § 102

Claims 1, 13, and 14 stand rejected by the Examiner under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Application Pub. No. 2005/10146346 to Kakizawa et at., hereinafter referred to as "Kakizawa". In particular, the Examiner contends that Kakizawa discloses a test switching circuit (DFT circuitry) for a high speed data interface of an integrated circuit comprising a plurality of switching transistors (**190**, **192**, **290**, and **292**) which switch in a test mode an integrated termination resistor output stage (termination resistors **132** and **134**) coupled to an output pad (transmitter pins **110** and **112**) of said integrated circuit in a data transmission signal path to an integrated termination resistor input stage (termination resistors **260** and **262**) coupled to an input pad (receiver pins **210** and **212**) of said

integrated circuit in a data reception signal path, wherein said plurality of switching transistors provide for a plurality of internal test signal paths between said input pad and said output pad (analog loop back paths **199** and **299**). The positions of the Examiner as summarized above with respect to claims 1, 13, and 14 are respectfully traversed as described below.

Claim 1 recites a switching circuit for a high-speed data interface of an integrated circuit comprising a plurality of switching transistors that switch in a test mode an integrated termination resistor output stage coupled to an output pad of the integrated circuit in a data transmission signal path to an integrated termination resistor input stage coupled to an input pad of the integrated circuit in a data reception signal path, wherein the plurality of switching transistors provide for a plurality of internal test signal paths between the input pad and the output pad.

It is respectfully submitted that Kakizawa does not disclose or suggest an integrated termination resistor output stage that can be switched (i.e., coupled and decoupled) to an output pad. Referring to Figure 1 of Kakizawa, the Examiner contends that transmitter pins **110** and **112** of Kakizawa serve as an output pad, but both transmitter pins **110** and **112** are *constantly coupled* to termination resistors **132** and **134**. Consequently, the teaching of Kakizawa does not allow a coupling and decoupling or switching of an integrated termination resistor output stage to an output pad by means of switching transistors.

Referring to Figure 2 of Kakizawa, the Examiner further contends that receiver pins **210** and **212** are regarded as input pads. Again, however, both receiver pins

210 and **212** are constantly coupled to termination resistors **260** and **262**. Consequently, Kakizawa again fails to disclose or suggest switching transistors for switching (hence, coupling and decoupling) an input pad to an integrated termination resistor input stage.

In addition, it is further respectfully submitted that Figures 1 and 2 of Kakizawa clearly teach *one single* "analog loop back path". Although Kakizawa discloses an analog loop back path **199** controlled by transistors **190** and **192** and an analog loop back path **299** controlled by transistors **290** and **292**, according to the teaching of Kakizawa, transmitter pins **110** and **112** are directly connected to the corresponding receiver pins **210** and **212**, respectively, in any self-test transmitter. (See, e.g., Kakizawa, paragraphs [0015] and [0021]) As a result, Kakizawa does not anticipate or render obvious that a plurality of switching transistors provide for *a plurality of internal test signal paths* between an input pad and an output pad of the high-speed data interface of an integrated circuit.

Regarding pending claims 13 and 14, it is respectfully submitted that the arguments presented with respect to claim 1 above apply equally to these claims. In particular, feature (c) of claim 13 recites the plurality of internal test signal paths and switching (i.e., coupling and decoupling) of an integrated termination resistor input stage and a termination resistor output stage. Likewise, feature (c) of pending claim 14 also recites a plurality of switching transistors for switching in a test mode the integrated termination resistor output stage to the integrated termination resistor input stage.

These features are neither taught nor suggested by Kakizawa, and thus it is respectfully submitted that the rejection of claims 1, 13, and 14 under 35 U.S.C. § 102(b) should be withdrawn and the claims and all claims depending therefrom should be allowed at this time.

Claim Rejection - 35 U.S.C. § 103

Claim 2 stands rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over Kakizawa in view of U.S. Patent No. 5,197,083 to Gandini et al., hereinafter referred to as "Gandini". Further, claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kakizawa in view of applicants' admitted prior art hereinafter referred to as "AAP". These rejections are likewise respectfully traversed.

As discussed above, Kakizawa fails to teach or suggest each and every element of independent claim 1. It is further respectfully submitted that Gandini does not remedy the deficiencies of Kakizawa. As a result, it is respectfully submitted that Kakizawa, taken either alone or in combination with Gandini, fails to teach or suggest every element of the test switching circuit of independent claim 1, in which a plurality of switching transistors switch an integrated termination resistor output stage coupled to an output pad to an integrated termination resistor input stage coupled to an input pad. Accordingly, because claims 2-4 depend upon claim 1, it is respectfully requested that the rejection of claims 2-4 under 35 U.S.C. § 103(a) also be withdrawn and the claims allowed at this time.

Allowed Claims

Applicants appreciate the Examiner's indication that claims 5-12 are allowable because none of the prior art discloses or fairly suggests a test switching circuit for a high speed data interface of an integrated circuit as is recited in these claims.

CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. 50-0426.

Respectfully submitted,

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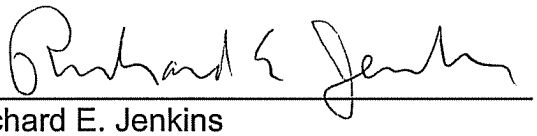
Date: March 18, 2009 By: 

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